second insulating layer, a wiring formed on said second insulating layer to electrically connect said external connect terminals to said circuit electrodes of said semiconductor device, and a third electrically insulating layer formed on said second insulating layer and on said wiring, wherein said second insulating layer contains particles to control a shape of said second insulating layer.

37. A semiconductor apparatus according to claim 36, wherein said second insulating layer is a stress relaxation layer to relieve stress caused between said semiconductor device and a board on which the apparatus is to be mounted.

38. A semiconductor apparatus according to claim 26, wherein said particles are made of a same material as that of said second insulating layer.

39. A semiconductor apparatus according to claim 36, wherein said second insulating layer contains particles of an organic material.

40. A semiconductor apparatus according to claim 36, wherein said second insulating layer at least contains particles of an amide-imide resin, of an ester-imide resin, of an ether-imide resin, of a silicone resin, or an acrylic resin, of a polyester resin.

41. A semiconductor apparatus comprising a semiconductor device, having circuit electrodes aligned centrally of the semiconductor apparatus, a first electrically insulating layer formed on said semiconductor device, with said circuit electrodes being exposed from said first insulating layer, a second electrically insulating layer

formed on said first insulating layer, external connection terminals formed on said second insulating layer, a wiring formed on said second insulating layer to electrically connect said external connection terminals to said circuit electrodes of said semiconductor device, and a third electrically insulating layer formed on said second insulating layer and on said wiring, wherein said third insulating layer covers an upper surface and a side surface of each of said first insulating layer and said second insulating layer except where said external connection terminals and said wiring are connected to each other.

42. A semiconductor apparatus comprising a semiconductor device having circuit electrodes aligned centrally of the semiconductor apparatus, a first electrically insulating layer formed on said semiconductor device with said circuit electrodes being exposed from said first insulating layer, a second electrically insulating layer formed on said first insulating layer, external connection terminals formed on said second insulating layer, a wiring formed on said second insulating layer to electrically connect said external connect terminals to said circuit electrodes of said semiconductor device, and a third electrically insulating layer formed on said second insulating layer and on said wiring, wherein said second insulating layer contains means for controlling a shape of said second insulating layer.

43. A semiconductor apparatus according to claim 42, wherein said means for controlling a shape of said second insulating layer comprises particles formed in said second insulating layer.

44. A semiconductor apparatus according to claim 42, wherein said second

insulating layer includes means for relieving stress caused between said semiconductor device and a board on which the apparatus is to be mounted.

45. A semiconductor apparatus according to claim 43, wherein said second insulating layer includes means for relieving stress caused between said semiconductor device and a board on which the apparatus is to be mounted.

46. A semiconductor apparatus according to claim 42, wherein said particles are made of a same material as that of said second insulating layer.

47. A semiconductor apparatus according to claim 42, wherein said second insulating layer contains particles of organic material.

48. A semiconductor apparatus according to claim 42, wherein said second insulating layer at least contains particles of an amide-imide resin, of an ester-imide resin, of an ether-imide resin, of a silicone resin, or an acrylic resin, of a polyester resin.

49. A semiconductor apparatus according to claim 36, wherein said second insulating layer has a thickness of from 35 μm to 150 μm.

50. A semiconductor apparatus according to claim 36, wherein said second insulating layer is a printed layer of an insulating material containing particles, formed by use of a print mask.

51. A semiconductor apparatus according to claim 41, wherein said second insulating layer is provided to relax stress produced between the semiconductor apparatus and a substrate on which to mount the apparatus.

52. A semiconductor apparatus according to claim 41, wherein said second insulating layer has a thickness of from 35 μm to 150 μm.

53. A semiconductor apparatus according to claim 41, wherein said second insulating layer contains particles to controlling a shape of said second insulating layer.

54. A semiconductor apparatus according to claim 42, wherein said second insulating layer has a thickness of from 35 μm to 150 μm.

55. A semiconductor apparatus according to claim 42, wherein said second insulating layer is a printed layer of an insulating material containing particles, formed by use of a print mask.

56. A semiconductor apparatus according to claim 41, wherein said second insulating layer includes means for relaxing stress produced between the semiconductor apparatus and a substrate on which to mount the apparatus.

57. A semiconductor apparatus according to claim 41, wherein said second insulating layer has a thickness of from 35 μm to 150 μm.